BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Prior arts

(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **06268093 A**

(43) Date of publication of application: **22 . 09 . 94**

(51) Int. Cl **H01L 23/12**
H01L 23/50

(21) Application number: **04044280**

(22) Date of filing: **02 . 03 . 92**

(71) Applicant: **NEC CORP**

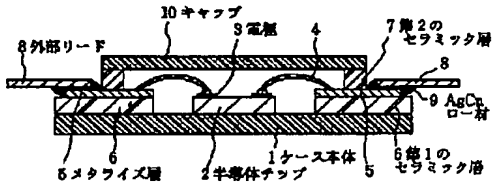
(72) Inventor: **HAYAKAWA YUKIO**

(54) **CERAMIC PACKAGE TYPE SEMICONDUCTOR DEVICE**

(57) Abstract:

PURPOSE: To reduce the size of a measuring jig and improve a high-frequency characteristic, by preventing a brazing material whereby an external lead is fastened on a metalized layer from protruding outward.

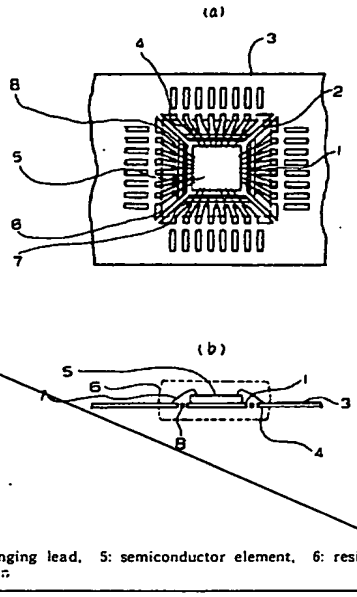
CONSTITUTION: On a main body 1 of a case, a semiconductor chip 2 and first ceramic layers 6 are fastened respectively, and a metalized layer 5 provided on the first ceramic layer 6 and an electrode 3 of the semiconductor chip 2 are connected by a bonding wire 4. Also, on the metalized layers 5, a cap 10 is put via second ceramic layers 7. On the other hand, external leads 8 are fastened on the metalized layers 5 via AgCu brazing materials 9 respectively. At this time, the metalized layer 5 is so formed as to be shorter than the first ceramic layer 6, or the external lead 8 is so formed that its end becomes wide, or a notch is so formed in the end part of the first ceramic layer 6 that a substantial recessed part is formed therein. Thereby, the protruding of the brazing material 9 is suppressed.



(54) SEMICONDUCTOR DEVICE
(11) 5-251609 (A) (43) 28.9.1993 (19) JP
(21) Appl. No. 4-83259 (22) 5.3.1992
(71) NEC KYUSHU LTD (72) MOTOAKI MATSUDA
(51) Int. Cl⁵. H01L23/50,H01L23/36

PURPOSE: To improve heat-dissipating properties of a semiconductor element by arranging a substance having a thermal conductivity higher than a sealing resin at a regular interval between an island and an inner lead.

CONSTITUTION: A high thermal-conductivity substance 8 is disposed among the side end of an island 1 and inner leads 4 faced oppositely to the side ends at a regular interval. Alumina, diamond, boron nitride, etc., having thermal conductivity higher than a resin 6 are used as the high thermal-conductivity substance 8. The high thermal-conductivity substance 8 is formed in the same thickness as the thickness of a lead frame 3 with the surface of the substance 8 being arranged, but the high thermal-conductivity substance 8 is formed in thicker size so far as it is not brought into contact with a small-gage wire 7. The substance 8 can also be projected from the top face of the island 1. Accordingly, the flow of heat transmitted over the inner leads from a semiconductor element is promoted, thus improving the heat-dissipating properties of the semiconductor element.

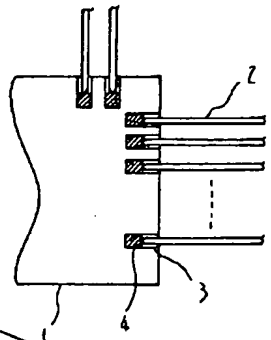


2: hanging lead, 5: semiconductor element, 6: resin sealing section

(54) PLAT PACK IC PACKAGE
(11) 5-251610 (A) (43) 28.9.1993 (19) JP
(21) Appl. No. 4-49070 (22) 6.3.1992
(71) NEC CORP (72) TADASHI TAKIZAWA
(51) Int. Cl⁵. H01L23/50,H01L21/66,H01L23/15

PURPOSE: To apply a power supply and a signal to an IC chip at a shortest distance, and to measure IC electrical characteristics excellently by forming a test pad while being connected to the lead brazing section of the ceramic board of a flat pack IC package.

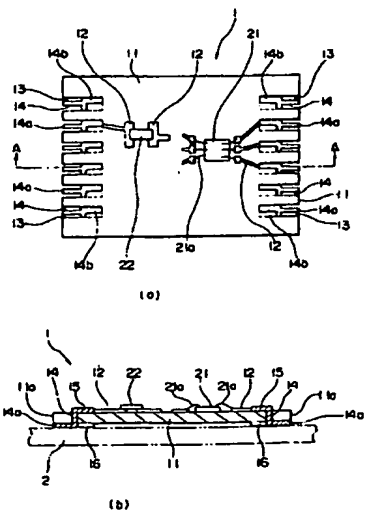
CONSTITUTION: Pads 3 for brazing to connect leads 2 are arranged onto the ceramic board 1 of a flat pack IC package and a test pad 4 onto the extension of the pads 3 for brazing. The test pad 4 is made slightly longer than the brazing sections 3 in order to be able to zigzag dispose a test probe. Accordingly, power supply and a signal can be applied to an IC chip or the test probe can be connected to the IC chip via a shortest distance, L and C components by lead length and generation of noises are prevented, and electrical characteristics can be measured excellently.



(54) HYBRID IC
(11) 5-251612 (A) (43) 28.9.1993 (19) JP
(21) Appl. No. 4-84839 (22) 6.3.1992
(71) SONY CORP (72) SEIICHI KOIKE
(51) Int. Cl⁵. H01L23/50

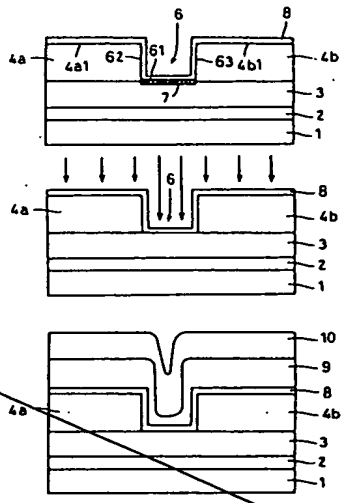
PURPOSE: To enable the surface mounting to the top face of a mother board of a hybrid IC by composing an upper terminal of a fitting section divided into a lower terminal and a front end section led out in approximately parallel with a substrate and holding the substrate by the upper terminal and the lower terminal.

CONSTITUTION: A plurality of notch sections 13 are formed to the peripheral section of a substrate 11, and leads 14 are set up into the notch sections 13 respectively. The leads 14 are constituted of fitting sections 14b divided into upper terminals 15 and lower terminals 16 and front end sections 14a led out in approximately parallel with the substrate 11. The substrate 11 is held among the upper terminals 15 and the lower terminals 16, and the upper and lower terminals are connected positively to the substrate 11 through soldering, etc. The front end sections 14a of the leads 14 are arranged under the state, in which the front end sections 14a are positioned on the sides farther inner than the side faces 11a of the substrate 11, and prevent projection toward the outside from the side faces 11a. Accordingly, the application of external force is prevented to an hybrid IC, thus allowing surface mounting to a mother board.



1: hybrid IC, 2: mother board, 12: wring pattern, 21: semiconductor element, 22: chip part, (a): plan view, (b): A-A line view sectional drawing, 21a: bonding wire

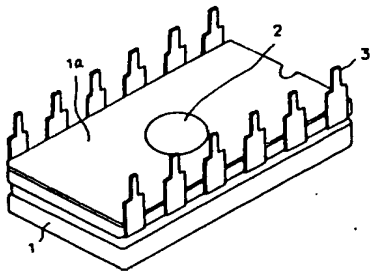
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
(11) 4-188852 (A) (43) 7.7.1992 (19) JP
(21) Appl. No. 2-318916 (22) 22.11.1990
(71) MITSUBISHI ELECTRIC CORP (72) TATSURO OKAMOTO
(51) Int. Cl⁵. H01L21/90,H01L21/3205



PURPOSE: To enhance wiring layers in adhesion to each other and to lessen an interface between the wiring layers in contact resistance by a method wherein ions are implanted into a second wiring layer formed on the base of a hole provided to an insulating layer formed on the first wiring layer through an ion implanting method.

CONSTITUTION: Ions are implanted into a second wiring layer 8 formed on the base 61 and the side faces 62 and 63 of a viahole 6 and the surfaces $4a_1$ and $4b_2$ of interlaminar insulating films 4a and 4b through an ion implanting method, whereby a first wiring layer 3 and the second wiring layer 8 are made to mingle with each other at an interface between them. By this setup, a second insulating film 7 is broken down by the implanted ions, an excellent interface is formed between the first wiring layer 3 and the second wiring layer 8, the adhesion between a third wiring layer 9 deposited on the second wiring layer 8 and the first wiring layer 3 is enhanced, and a contact resistance between them can be reduced to a value small enough.

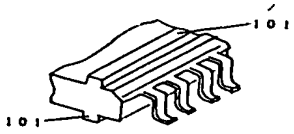
(54) PACKAGE
(11) 4-188853 (A) (43) 7.7.1992 (19) JP
(21) Appl. No. 2-318893 (22) 22.11.1990
(71) MITSUBISHI ELECTRIC CORP (72) MUNEHIRO YOSHIDA
(51) Int. Cl⁵. H01L23/02

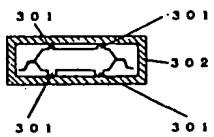


PURPOSE: To protect data written in a semiconductor memory element without providing a data protecting means by a method wherein a window through which the semiconductor memory element is irradiated with ultraviolet rays or the like is provided in the surface of a package opposite to the mounting member for the package.

CONSTITUTION: In a package 3 which houses a semiconductor memory device whose written data are erased by the irradiation with ultraviolet rays or the like, an IC incorporating the memory element is mounted on a mounting member such as an printed wiring board or the like (not shown in a figure) of the package 1 through such a manner that lead wires 3 are soldered to lands formed on the mounting member, and a window 2 is covered with the mounting member. Therefore, external penetrating light such as direct sunlight incident on the window 2 can be blocked by the mounting member, and the data written in the memory element can be erased by irradiating it with ultraviolet rays through the window 2, so that a package can be obtained which can dispence with a means which is used for protecting data against external light which penetrates through the window 2.

(54) SEMICONDUCTOR DEVICE
(11) 4-188854 (A) (43) 7.7.1992 (19) JP
(21) Appl. No. 2-318796 (22) 22.11.1990
(71) SEIKO EPSON CORP (72) HIROTAKA TANAKA
(51) Int. Cl⁵. H01L23/28





PURPOSE: To lessen semiconductor devices in fraction defective caused by static electricity by a method where a rail-shaped protrusion is provided to the front or the rear of a package.

CONSTITUTION: A semiconductor device is inserted into a packaging magazine tube 302, where only one or more rail-shaped protrusions 101 and 301 provided to the front or the rear of the package of the semiconductor device are brought into contact with the inner wall of the tube 302. Therefore, if the semiconductor device is inserted into the tube 302 once, the rubbing of the package against the tube 302 caused by play can be reduced to the irreducible minimum, so that the charge by frictional electricity can be remarkably lessened in quantity, and a semiconductor device can be lessened in fraction defective caused by static electricity.

55-86186

Title of The Invention: Electronic component and the mounting method thereof

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to a mounting technique of a small electronic component, more particularly to a mounting technique of a resin-molded transistor onto a wiring board.

As for a technique for mounting a small resin-sealed transistor on a printed board for connecting the transistor to wirings in an adequate position, a tentative-placement/soldering method is widely used for its simplicity.

According to this method, as shown in Fig. 1A, an adhesive 2 is applied on a printed board 1 in advance through potting or printing etc., and thereon, as shown in Fig. 1B, the resin body 3 of the transistor is half-fixed with its leads 4 contacting to wirings 3 on the board, and then the transistor is connected to the printed wirings by solder 6 that has been applied to the leads in advance to achieve mounting as shown in Fig. 1C. This method, however, has the following drawback.

In a case of an electronic component such as the transistor whose connecting terminals (leads) are attached at once via soldering etc. to a plane surface of a ceramic or resin

constituting an insulating substrate for the printed wirings, after mounting, a cavity 7 is formed between the substrate and an insulator case such as a sealing resin body etc. by burning out the adhesive in a furnace as shown in Fig. 1C. This cavity, as priorly explained, is used as an adhesion margin on which the adhesive is applied for the tentative placement of the electronic component on the substrate. However, when considering a heat dissipation capability during operation of the semiconductor device, the heat dissipation from the insulator case to the substrate is substantially inhibited by this cavity. Recently, it is strongly demanded due to the growing demands for further integration of electronic circuits, and miniaturization of outer dimensions without degrading its output is being required. Accordingly, how the heat dissipation may be improved is the issue that needs to be addressed.

The present invention was invented with an intention to solve the above-described problem of the prior art, and an object thereof is to provide an electronic component whose heat dissipation capability is improved by bringing the bottom surface of an insulator case such as a resin body into close contact with a substrate surface, and a mounting method thereof.

According to one aspect of the present invention for achieving the above object, in an electronic component having

a plurality of leads 4 drawn out from side surfaces of a main body 3, as shown in Fig. 2(a), part of the bottom surface of the main body includes planes 8 which form given gaps 8 between them and a mounting plane X-X, while the rest of the part forms a plane 9, which protrudes so as to match with the mounting plane X-X.

Another aspect of the present invention is a mounting method of the aforementioned electronic component on a printed board, the method comprising the steps of, with reference to 2A-2C of Fig. 2; 2A selectively applying an adhesive 10 onto given locations of a wiring board 1 to which the main body of the aforementioned electronic component is attached; 2B placing the flat concave portions 8 in the bottom of the main body of the electronic component over the locations on which the adhesive has been applied, and leaving it aside or baking it until the main body is tentatively affixed to the substrate; and thereafter, 2C connecting each lead 4 to a wiring 5 of the substrate by solder 11.

According to the present invention as described in relation to the above embodiments, the adhesive used between the main body of the electronic component and the wiring board surface is located at a part of the bottom of the main body, and after the substrate is cleaned, cavities are present only partially as shown in Fig. 2C, and the flat protrusive part of the bottom is affixed in close contact with the substrate,

so that the heat dissipation effect is substantially improved. For instance, when it was applied to a small resin-sealed transistor of H3mm x W1.5mm x D1mm as an electronic component, the maximum collector loss was found to be improved from 180mW to 230mW as a result of an experiment.

The above exemplary electronic component mounting method of the present invention has been described as being a manufacturing method of a hybrid IC comprising the steps of; tentatively attaching the semiconductor device→soldering the leads→cleaning the substrate, however, the same effect may be expected even when a electronic component according to the present invention is mounted to a substrate only by soldering using a soldering iron without the use of an adhesive.

Besides the resin-sealed transistor described in the embodiments, the electronic component of the present invention may be implemented as any electronic components including can-sealed type and ceramic package-sealed type semiconductor devices (transistors, diodes, IC's), capacitors, and resistors. Furthermore, the present invention may similarly be applied to electronic components of various shapes, for example, those shapes that are illustrated in Fig.3A - 3F, Fig. 4, Fig. 5A - 5F, and Fig. 6A - 6D, respectively.

63-191651

Title of The Device: Semiconductor device

2. SCOPE OF CLAIM

A semiconductor device, in which leads connected to electrodes of a semiconductor element accommodated within a package are jutting out from mid-sections in a height direction of an outer side surface of the package, wherein a portion of the outer side surface of the package located on the lower side of the lead-jutting sections is adequately located inwardly relative to a portion of the outer side surface located on the upper side.